information for each executive memory and confirms whether or not a capacity adequate for a transfer is available.

In the case that the capacity of any one among the executive memories is inadequate, in order to guarantee a capacity that will allow the transfer, the control unit 40 initializes the executive memories in step 5B, and erases all of the stored data. Specifically, initializing the executive memories means initializing the control information of each control memory. At this time, all of the pattern files stored therein appear to be erased.

Next, in step 5C, the control unit 40 again transfers the pattern files to be used in the test of the semiconductor to the executive memories, and after completing the transfer of the pattern files, begins the test of the semiconductor based on the pattern data in step 5D.

The transfer of the pattern files and the initialization of the executive memories are repeated, and the tests using all of the pattern files are carried out according to the file control algorithm for the executive memory that has been described above.

However, once transferred to the executive memories, all of the pattern files necessary for the test are transferred to the executive memories so that they can be managed as the pattern files until the initialization of the executive memories, and thereby after the second test, initialization of the executive memories and further transfers are not necessary, and the load during execution is reduced.

Furthermore, in recent years, in the testing of semiconductors, the test items and the test content has greatly increased due to the increased number of functions of the semiconductor itself, and the pattern files for the tests have become very large, there are few tests of semiconductors that can transfer all of the pattern files to the executive memory, the transfer of pattern files is repeated more than two times during the test, and

thereby the efficiency of the test of the semiconductor deteriorates.

In addition, in the conventional semiconductor apparatus, the pattern files used in the test are transferred to the executive memories according to the order of execution of the test items irrespective of the frequency of use, and furthermore, in the case that there is insufficient free memory capacity, the simple algorithm of initializing all memory is used, and thus there is the drawback that high speed testing cannot be carried out.

This means that in order to provide a high speed test environment under the condition that the amount of data of the pattern files necessary for testing the semiconductor may exceed the memory capacity of the executive memory because the capacity of the executive memory is limited, an algorithm is required that retains the pattern files that are used with a high frequency in the executive memory, and that reduces to a minimum the pattern files that are transferred a plurality of times.

Generally, the testing of semiconductors uses a method wherein a semiconductor is categorized as defective in the case that even one among the many test items fails, and in consideration of the throughput of the testing, the test is discontinued when any test item fails, and the test of the next semiconductor is begun.

Therefore, the frequency of use of a pattern file can change depending on the defect rate for each semiconductor, and thus uniformly assigning an algorithm that decides the frequency of use of a pattern file in the semiconductor test apparatus is difficult.

In consideration of the background described above, it is an object of the present invention to provide a semiconductor test apparatus that reduces to a minimum the number of the internal transfers of pattern files, and can reduce the testing time of the semiconductor.

SUMMARY OF THE INVENTION

The semiconductor test apparatus according to the present invention tests the operation of a semiconductor based on a plurality of pattern data and is characterized in comprising a counter device that counts the number of times pattern data is used for each pattern file and a control unit that produces a pattern file use frequency table showing the relationship between each of the files and the number of times the files are used, and stores this pattern file use frequency table in the memory.

The semiconductor test apparatus of the present invention is characterized in that the counting device counts the number of times pattern data is used in the test of a preset number of semiconductors.

The semiconductor test apparatus of the present invention is characterized in that the control unit loads the pattern files in descending order of the use frequency table after producing the pattern file use frequency table.

The semiconductor test apparatus of the present invention is characterized in that the control unit deletes the pattern files beginning with those having a low use frequency in the case that the capacity of the executive memory is in sufficient when transferring pattern files to the executive memories.

The control method of the semiconductor test apparatus of the present invention that tests the operation of a semiconductor based on a plurality of pattern data is characterized in providing a counting step in which the number of times pattern data is used is counted for each pattern file and a storage step in which a pattern file use frequency table that shows the relationship between each file and the number of times this file is used, and stores this pattern file use frequency table in the memory.

The control method of the semiconductor test apparatus of the present invention